

Low-Cost Robust Thermal Solution for High Power AI/Datacenter Processors

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Abstract—High-power AI and high-performance computing (HPC) processors now routinely operate at heat fluxes exceeding 1 W/mm^2 , making thermal interfaces and lid design critical system bottlenecks [1], [2]. While advances in transistor density and chiplet integration have significantly improved computational throughput, they have also intensified thermal non-uniformity, hotspot severity, and thermo-mechanical reliability risks [2]. This study systematically evaluates candidate thermal interface materials (TIMs) under realistic die-to-lid conditions, emphasizing bondline thickness (BLT), contact resistance, manufacturability, and long-term reliability for large-scale data-center deployment [1]. A qualitative cost–performance matrix is developed to guide material selection. The selected TIM solutions are then coupled with a lid-material trade study that balances thermal spreading capability against coefficient of thermal expansion (CTE) mismatch with silicon. Finally, multiple lid geometries are assessed using CAD-based thermo-mechanical co-simulation to quantify warpage reduction and temperature distribution [1]. Results indicate that PCM-based TIMs and thixotropic greases provide the best system-level balance, while Cu-Mo and vapor-chamber lids offer complementary reliability- and performance-driven solutions for next-generation AI data centers.

Keywords— thermal interface materials, bondline thickness, AI processors, lid design, thermal spreading, CTE mismatch

I. INTRODUCTION & OBJECTIVE

The rapid expansion of artificial intelligence workloads has driven processor package power beyond 300–1200 W, with localized heat flux frequently exceeding 1 W/mm^2 [1], [2]. Unlike conventional consumer electronics, AI and HPC processors operate continuously and experience repeated thermal cycling due to workload scheduling, power capping, and maintenance states [9]. Typical temperature swings of 60–80 °C exacerbate both thermal resistance sensitivity and thermo-mechanical fatigue [1].

Poor thermal management leads to elevated junction temperatures, accelerated material degradation, performance throttling, and increased operational expenditure [2], [10]. Furthermore, modern chiplet-based architecture introduces non-uniform power density, creating localized hotspots that dominate system reliability rather than average temperature [1], [10].

The objective of this work is to identify a low-cost, robust thermal solution for AI and datacenter processors by:

1. Screening and benchmarking candidate TIMs under realistic heat-flux conditions
2. Identifying process methods that minimize TIM thermal impedance and variability
3. Evaluating lid materials that balance thermal spreading and CTE compatibility
4. Validating lid concepts through thermo-mechanical co-simulation [1]

II. SCREENING & BENCHMARKING OF THERMAL INTERFACE MATERIALS

A. Role of TIMs in AI Processor Packaging

Although mating surfaces may appear smooth macroscopically, direct solid-to-solid contact typically accounts for less than 20% of the apparent interface area [3]. Trapped air pockets, with thermal conductivity approximately $0.026 \text{ W/m}\cdot\text{K}$, dominate interface resistance unless displaced by a compliant TIM. TIMs therefore form the primary thermal conduction path between the silicon die and the integrated heat spreader (IHS) or lid.

The total interface impedance can be expressed as:

$$Z_{total} = R_{c,1} + \frac{BLT}{kA} + R_{c,2}$$

Where BLT is the bondline thickness, k is the bulk thermal conductivity, A is the contact area, and R is the contact resistance. In practice, BLT variability and contact resistance frequently dominate over bulk conductivity, particularly for BLT below $50 \mu\text{m}$ [3], [4].

B. TIM Categories Evaluated

Six TIM categories were screened based on maturity and relevance to high-power AI packaging:

- Thermal greases
- Phase-change materials (PCMs)
- Solder-based TIMs
- Sintered silver
- Liquid metals
- Advanced composite TIMs [1]

These categories span a wide range of thermal performance, compliance, rework ability, and cost.

C. Process Factors Affecting TIM Impedance

Wetting & Asperity Filling - Effective wetting is essential for minimizing contact resistance by displacing air trapped within surface asperities [4]. Poor wetting leaves insulating voids that significantly increase total thermal impedance.

Specific Gravity & Pump-out Resistance - TIMs are procured by mass but applied by volume. Higher density and viscosity generally improve resistance to pump-out under sustained clamping load and thermal cycling.

Strain-Rate-Dependent Rheology - Many TIMs exhibit thixotropic behavior, flowing readily during dispensing but stiffening under static conditions. This behavior is quantified by the thixotropic index,

$$TI = \frac{\eta_{low}}{\eta_{high}}$$

Where higher values indicate improved bondline stability [1].

D. Bondline Thickness Control

BLT is the dominant contributor to TIM thermal resistance. Reducing BLT proportionally reduces bulk resistance; however, excessively thin or non-uniform bondlines increase mechanical risk and pump-out susceptibility [3], [5], [8].

Effective BLT control methods include:

- Uniform pressure application using spring-loaded fasteners
- Spacer beads (10–100 μm) to enforce minimum BLT [8]
- Precision pick-and-place assembly for low-tolerance interfaces [5]

These techniques are broadly applicable across TIM categories and are essential for large-scale manufacturing repeatability.

E. Cost-Performance Matrix & Selection

A qualitative matrix was developed using the following criteria: thermal resistance, BLT controllability, manufacturability, serviceability, reliability risk, and total cost [10].

Key observations include:

- High thermal conductivity alone does not guarantee low interface impedance
- Thixotropic greases and PCMs exhibit superior pump-out resistance
- Curable systems improve stability but reduce rework ability

Based on this analysis, PCM-based TIMs and thixotropic greases were selected as baseline candidates for further system-level evaluation [1], [14].

III. CURRENT THERMAL MANAGEMENT

A. The Background, Problems & Challenges of Current Thermal Management

With the rapid advancement of AI workloads, processor complexity and power density have increased dramatically. For example, the AMD Ryzen 7 1700 (2017) integrates 4.8 billion transistors, while the NVIDIA A100 (2020) features 54 billion, an 11.25 $\times$ increase, intensifying thermal challenges [1], [9]. Poor thermal management can lead to:

- Hardware degradation and downtime
- Performance bottlenecks
- Higher operational costs [2]

Modern HPC processors generate substantial heat and exhibit non-uniform temperature distributions, creating localized hotspots. Advanced chiplet packaging further increases power density and thermal constraints. Consequently, AI data centers face:

- Increased heat density
- Energy efficiency
- Hotspots and uneven temperature distribution

The lid must address two fundamental issues:

1. Heat is generated locally, but must be removed globally
2. Materials expand differently when heated

Problem 1: Heat is generated locally, but must be removed globally

Modern AI/HPC processors integrate tens of millions to trillions of transistors, which use large monolithic or chiplet-based dies, which contain non-uniform activity regions (matrix engines, HBM interfaces, and AI accelerators)

As a result, the power density of the AI/HPC processors is highly non-uniform. Also, the local heat flux routinely exceeds 1 W/mm² [1]. The hotspots also constrain the system's reliability and performance.

Therefore, it is the peak junction temperature, not the average temperature, that determines throttling and system lifetime.

Problem 2: Materials expand differently when heated

As seen in Table 1, silicon exhibits a low coefficient of thermal expansion (CTE), whereas metallic lids expand significantly, making CTE mismatch unavoidable [1], [6]. Unlike consumer electronics, AI and data-center processors operate continuously and experience load-driven power fluctuations, resulting in thermal cycling with typical temperature swings of 60–80 °C, and even higher at localized hotspots. During heating, the lid attempts to expand laterally, while the silicon die constrains this motion due to its lower CTE, forcing deformation at the interfaces. This induces global package warpage, shear stress in TIM layers, and peel stress at die corners—the most failure-prone regions [1]. Over time,

these effects can cause TIM pump-out, interfacial delamination, increased thermal resistance, and accelerated fatigue, ultimately compromising system reliability.

B. Thermal Spreading V.S. CTE Match

The major issue with these two problems is that they are **mutually exclusive** (i.e., they conflict). In other words, the materials that best solve thermal spreading typically worsen CTE mismatch, while materials that reduce CTE mismatch often degrade thermal spreading [2].

To simplify the mechanism behind this phenomenon:

- High thermal conductivity $\rightarrow$ metals $\rightarrow$ high CTE
- Low CTE $\rightarrow$ ceramics/refractory materials $\rightarrow$ lower k

The lid simultaneously acts as a thermal spreader to suppress localized hotspots and as a mechanical intermediary that must absorb or mitigate thermally induced strain caused by CTE mismatch between silicon and the cooling structure [1].

C. Lid Materials Evaluation

Cu:

- Thermal spreading: strong (high k)
- CTE match: poor vs Si (16.5 vs 2.6) $\rightarrow$ higher warpage/stress risk
- Best use: when cost is king, and you manage warpage via geometry, stiffness control, preload, and good TIM bondline control [1].

Cu-alloy:

- Thermal: slightly worse than Cu (k down)
- CTE: similar to Cu (still mismatch)
- Best use: when you need strength/hardness (less denting, better flatness retention) and accept a modest thermal penalty [1], [10], [11].

Cu-Mo:

- Thermal: moderate (lower than Cu) but acceptable for high power if thickness/area optimized
- CTE: much better tunability, can land closer to ceramics/substrates, and reduce warpage
- Best use: when reliability/warpage dominates, and you can pay more per lid [1].

Vapor chamber lid

- Thermal spreading: potentially best by far (effective k can exceed 5000 W/m $\cdot$ K for spreading)
- CTE: usually copper envelope $\rightarrow$ CTE still $\sim$ Cu; mechanical benefit is not CTE match, it's thermal flattening (lower gradients)
- Best use: when hotspot control is the bottleneck and manufacturing/reliability risks are acceptable and mitigated (design + QC) [1].

TABLE I. KEY COEFFICIENTS OF THERMAL EXPANSION (CTE) OF MAJOR LID MATERIALS.

Material	CTE (ppm/K)
Silicon	$\sim$ 2.6
Copper	$\sim$ 16-17
Aluminium	$\sim$ 23
Cu-Mo (engineered)	$\sim$ 6-10

TABLE II. THERMAL SPREADING VS. CTE OF MAJOR MATERIAL CANDIDATES.

Candidate	Thermal Spreading	CTE/Warpage	Mfg Risk	Cost	Expected Positioning
Cu	High	Weak	Low	Low	"Baseline"
Cu Alloy [10]	Med-high	Weak	Low	Low	"Practical baseline"
Cu-Mo	Medium	Strong (tunable)	Med	High	"Reliability pick"
Vapor chamber	Very high (effective k)	Medium	High	Med	"Performance pick"

TABLE III. THERMAL & MECHANICAL ROLES OF MAJOR LID MATERIALS.

Lid Type	Thermal Role	Mechanical Role
Cu	Maximize spreading	High stress risk
Cu Alloy [10]	Balance spreading + strength	Slightly improved durability
Cu-Mo	Acceptable spreading	Strong warpage control
Vapor chamber	Extreme spreading	Stress reduction via ΔT flattening

IV. LID THERMAL-STRUCTURAL CO-SIMULATION

A. Background of Co-Simulation

As discussed in Section 2.2.1, CTE mismatch between the chip and substrate is the primary cause of reliability issues in flip-chip packages, leading to excessive warpage under thermal loading. Effective warpage control is therefore the priority, alongside substrate area reduction to manage cost [11]. In addition to stiffener rings, lid design is a key mitigation strategy and the focus of this work. In capped-die flip-chip packages, a metal lid bonded to the die via adhesive increases the effective CTE of the die, thereby reducing thermomechanical stress [6].

Thermal interface materials (TIMs) further play a critical role by filling microscopic air gaps and establishing a continuous heat-conduction path. For modern HPC chips operating at 300–1200 W and heat fluxes exceeding 1 W/mm², even an additional 0.01–0.05 $^{\circ}\text{C}\cdot\text{cm}^2/\text{W}$ of interface resistance can increase junction temperature by 10–20 $^{\circ}\text{C}$, exacerbating hotspots and throttling risk [1]. However, cyclic thermal expansion can induce TIM displacement, which must be considered in lid optimization. Optimal lid design can be achieved through adjustments in geometry, thickness, and material selection, enabling effective CTE matching between

the capped die and substrate and ultimately achieving warpage-free packaging.

TABLE IV. SPECIFIC DATA FOR COMMON LID MATERIALS.

Property	Pure Copper (Cu)	Copper Alloy (Cu-W, Cu-Cr-Zr) [11]	Cu-Mo Composite	Vapor Chamber (Cu-based)
Thermal Impedance ($^{\circ}\text{C}\cdot\text{cm}^2/\text{W}$)	$\sim 0.002\text{--}0.005$	$\sim 0.003\text{--}0.006$	$\sim 0.004\text{--}0.008$	$\sim 0.001\text{--}0.003$
Thermal Resistance (K/W)*	$\sim 0.01\text{--}0.03$	$\sim 0.015\text{--}0.04$	$\sim 0.02\text{--}0.05$	$\sim 0.005\text{--}0.02$
Typical Thickness (mm)	1.0–2.5	1.0–2.5	1.5–3.0	2.0–4.0
Thermal Conductivity ($\text{W}/\text{m}\cdot\text{K}$)	$\sim 390\text{--}400$	250–330	180–230	Effective $\kappa > 2000$
CTE (ppm/K)	$\sim 16.5\text{--}17$	12–15	7–9	~ 17 (Cu shell)
Density (g/cm^3)	8.96	8.5–9.2	9.5–10.2	$\sim 6\text{--}7$ (effective)
Key Advantages	Excellent thermal spreading; low cost; easy machining	Improved strength; reduced warpage vs Cu	Excellent CTE match to Si; low stress	Exceptional lateral heat spreading; hotspot mitigation
Key Limitations	Large CTE mismatch with Si; warpage risk	Lower κ than pure Cu; higher cost	Lower thermal spreading; expensive	Cost; thickness; reliability validation
Typical Applications	Mainstream CPU/GPU lids	High-power CPUs; enterprise GPUs	AI accelerators; large dies	Ultra-high-power AI / HPC lids

B. Reasons for Approach & Chosen Techniques

To identify the most effective and accurate way to present the results, the team analyzed prior research on related topics.

Possible approaches include:

- Using a Cartesian coordinate system, XYZ, comparing the warpage displacement with respect to different dimensions and material properties.
- Using FEM (Finite Element Method) software, such as ANSYS, to conduct numerical simulations and thermal analyses.

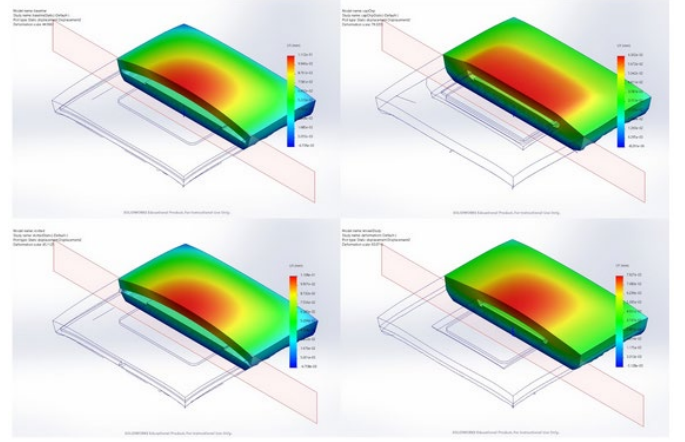


Fig. 1 Simulation results (Y (def)), baseline (top left), cap (top right), slotted (bottom left), stiffener (bottom right).

- Using SolidWorks to construct various lid design 3D models and conduct thermal analyses using its simulation capabilities.

The team members chose SolidWorks because they have extensive experience in 3D design and CAD with this software. They also used SolidWorks simulation to compare the lid's warpage, hot-spot, and temperature-distribution dimensions.

The team did not use the XYZ Cartesian coordinate system due to the few parameters, such as the lid size and wall thickness. Moreover, due to limited access to professional software such as ANSYS, they could not collect sufficient data to generate a graph in the XYZ Cartesian coordinate system.

The team set up a SolidWorks Thermal and Static Simulation to test the lid designs. In the Thermal Simulation setup, a convection of $1000 \text{ W}/\text{m}^2$ with a bulk ambient temperature of 298.15 K was applied to the top surface of the lid. Additionally, 250 W of Heat Power was applied to the top face of the die [1]. An initial temperature of 25°C was added to the simulation and a generalized thermal resistance of $0.005 \text{ K}/\text{W}$ was simulated between the die and the lid to simulate the TIM.

The substrate was modeled as a $50 \times 50 \times 1.5 \text{ mm}$ block fabricated out of PEEK. A $25 \times 32 \times 0.7 \text{ mm}$ die of Silicon was used alongside a Copper lid.

V. COMPARISON OF COOLING SYSTEMS

To manage the thermal challenges of AI data centers, the AI industry is adopting and developing several innovative cooling strategies. The major cooling strategies include air cooling and liquid cooling [2].

A. Air-based Cooling Systems: Dominance in Ubiquity

Air cooling uses fans and heat sinks to dissipate heat from HPC chips and remains the most widely deployed data-center cooling method due to its low cost, simplicity, and minimal infrastructure requirements [2].

TABLE V. SIMULATION RESULTS OF DIFFERENT LID DESIGNS.

Name	Max Deformation (mm e-2)	Minimum Deformation (mm e-2)	Average Deformation (mm e-2)	Warpage (Max - Min) (mm e-2)
Baseline Study	10.28	0.9352	6.212	9.35
Capped Lid	5.332	4.542	5.076	0.79
Slotted Lid	10.24	0.9370	6.162	9.303
Stiffener Lid	7.001	1.419	4.636	5.582

TABLE VI. COMPARISON OF CURRENT AIR, LIQUID, AND HYBRID COOLING SYSTEMS.

Attribute	Air Cooling	Hybrid Cooling	Liquid Cooling
Typical Technologies	CRAC, CRAH, Free Air, Evaporative	RDHx, CoolPhase Flex, Cool Array	DLC, Immersion, Spray, Jet
Rack Density	≤ 40 kW	40 - 100 kW	≥ 250 - 300 kW
Efficiency (PUE)	1.15–2.0	1.25–1.33	1.02–1.10
Water / Heat Reuse	Low–moderate; climate-dependent	Partial reuse; low WUE	High reuse; 40–55 °C
Key Strength	Low cost; mature; simple	Retrofit-friendly; scalable	Highest efficiency; hotspot control

B. Liquid-based Cooling Systems: High Efficiency & Future Development Potentials

Liquid cooling provides superior thermal performance for high-density hardware compared with air cooling, offering higher heat transfer efficiency, lower energy consumption, and greater heat-reuse potential [2], [7]. Direct Liquid Cooling (DLC) is the most mature approach, using cold plates on high-power components and enabling energy reductions of up to 72.4%, but high cost, maintenance complexity, and leakage risk limit adoption, with over 60% of data centers still relying on air cooling. Immersion cooling delivers higher cooling capacity but remains niche due to cost and operational barriers. Emerging methods such as spray and jet impingement cooling target extreme heat flux applications.

C. Hybrid Cooling Systems: Market Adoption & Middle Ground

Hybrid cooling systems provide a cost-effective transition between air and liquid cooling, enabling higher rack densities while preserving existing infrastructure [2].

VI. THERMAL-STRUCTURAL CO-SIMULATION AND OPTIMIZATION

To proof thermomechanical reliability at the system level, a co-simulation was performed by integrating the package, motherboard (FR-4), and retention mechanism. To accurately represent the compliance of the BGA interconnect layer without the computational cost of modeling thousands of individual spheres, an 'Effective Elastic Modulus' was applied to the solder layer volume. Following the Rule of Mixtures approximation for a typical BGA area density of 20%, the modulus of the solder block was reduced to 2.0 GPa [1]. This ensures the stiffness ratio between the solder array and the underfill encasement accurately reflects physical reality.

The Lid-to-Substrate interface was modeled as 'Bonded' for both thermal and structural analysis. While this simplifies the thermal resistance of the adhesive sealant, the low thermal conductivity of the underlying FR-4 substrate (0.3 W/m·K) ensures that heat flow remains dominated by the primary conduction path through the IHS, validating this approximation for system-level trends [1].

A. Geometric Optimization through Design of Experiments

A baseline analysis was conducted on four lid geometries to assess the impact of lid stiffness on solder stress before the application of underfill. The results confirmed the correlation: **Lower Warpage = Lower Stress**.

- **Baseline Study:** Exhibited the highest warpage ($\Delta \approx 9.35 \times 10^{-2}$ mm) and highest stress (81.75 MPa), confirming it as the least optimal design.
- **Capped Lid:** The "Capped" (Pedestal) geometry emerged as the geometric winner. Its thick center increased stiffness sufficiently to minimize bowing ($\Delta \approx 0.8 \times 10^{-2}$ mm), effectively keeping the motherboard flat and reducing shear force on the solder balls. This design achieved a ~14% reduction in stress compared to the baseline (70.21 MPa vs 81.75 MPa) [1].

While the Capped Lid reduced stress by ~14%, the peak stress of 70.21 MPa remained significantly higher than the yield strength of the Indium solder (≈ 2 MPa). This confirmed that geometric optimization alone is insufficient for reliability, necessitating the use of Underfill [1].

TABLE VII. POST-UNDERFILL STRESS RESULTS (RELIABILITY VALIDATION), WITH THE CAPPED DESIGN (BOLDED TEXT) THE BEST.

Design Variant	Max Stress (MPa)	Avg Stress (MPa)	Improvement vs. Non-Underfilled
Baseline	32.85	15.07	59.8%
Capped	25.10	10.56	64.2%
Slotted	26.68	14.91	66.3%
Stiffener	30.86	14.28	61.0%

B. Reliability Enhancement via Underfill

To mitigate the critical stress levels, an epoxy underfill ($E=10$ GPa) was modeled. As described by Fan et al., underfill creates a rigid coupling between the die and substrate, redistributing thermomechanical stress away from the fragile solder joints into the epoxy matrix [1], [6], [12].

C. Final Reliability Assessment

The simulation validated the literature, demonstrating a ~60% reduction in solder stress across all designs, proving that the underfill successfully bypassed the solder joints [1].

- **Optimal Design:** The Capped Lid remained the superior design, achieving the lowest system-level stress of 25.10 MPa.
- **Viable Alternative:** The Stiffener Lid performed comparably (26.68 MPa), presenting a cost-effective alternative if the manufacturing of the monolithic Capped Lid proves too costly.
- **Failure Analysis:** Although the peak Von Mises stress (25.1 MPa) theoretically exceeds the quasi-static yield strength of Indium (≈ 2 MPa), the 64% reduction in stress magnitude indicates a significant improvement in fatigue life [12].

In a real-world scenario, the Indium would undergo plastic deformation rather than brittle fracture; the underfill effectively prevents this deformation from exceeding critical strain limits, thereby proving thermomechanical reliability.

VII. CONCLUSION

This paper systematically evaluated thermal interface materials (TIMs) and lid geometries to combat the escalating thermal and mechanical challenges in high-power AI and HPC packages. From material benchmarking, geometric design, and system-level co-simulation, a three-stage optimization process yielded the following results:

- **Material Selection:** Benchmarking identified Phase Change Materials (e.g., Honeywell PTM7950) and Indium solder as the optimal interface baseline, balancing ultra-low thermal impedance ($0.04^\circ\text{C}\cdot\text{cm}^2/\text{W}$) with long-term pump-out resistance.
- **Geometric Optimization:** A Design of Experiments on lid geometry revealed the stiffness-optimized "Capped" pedestal lid proved superior to standard designs, reducing package warpage by 91% ($\Delta 9.35 \rightarrow 0.8 \times 10^{-2}$ mm) and lowering solder shear stress by ~14% purely through structural stability.
- **System-Level Reliability:** Co-simulation confirmed that underfill is mandatory for Indium interconnects. The application of a rigid epoxy ($E=10$ GPa) delivered a 64.2% reduction in peak stress, lowering it to 25.10 MPa.

While the final stress state exceeds Indium's static yield, the combination of the stiff Capped Lid and underfill reinforcement drastically minimizes the plastic strain energy density per cycle,

ensuring thermomechanical reliability for next-generation data center workloads.

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